IN THE CLAIMS

Please amend Claims 15-19 and 25-27 as follows.

1-14. (Canceled)

15. (Currently Amended) A power semiconductor device made in accordance with a method comprising the steps of:

A. providing a substrate of a first or second conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

2. forming at least one trench in said epitaxial layer said at least one trench having walls and a bottom;

3. depositing a barrier material along the walls of said trench;

4. implanting a dopant of a second conductivity type through the barrier material into a portion of the epitaxial layer adjacent to and beneath the bottom of said trench;

5. diffusing said dopant to form a first doped layer in said epitaxial layer;

6. removing the barrier material from at least the bottom of the trench;

7. etching the trench through said first doped layer and repeating steps (B.3) -- (B.6) to form a second doped layer vertically below said first doped layer;

8. depositing a filler material in said trench to substantially fill said trench;

9. diffusing said dopant in the first and second doped layers to cause the first and second doped layers to overlap one another; and

C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween.

16. (Currently Amended) A power semiconductor device made in accordance with a method comprising the steps of:

A. providing a substrate of a first or second conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

2. forming at least one trench in said epitaxial layer said at least one trench having walls and a bottom;

3. depositing a barrier material along the walls of said trench;

4. implanting a dopant of a second conductivity type through the barrier material into a portion of the epitaxial layer adjacent to and beneath the bottom of said trench;

5. diffusing said dopant to form a first doped layer in said epitaxial layer;

6. removing the barrier material from at least the bottom of the trench;

7. etching the trench through said first doped layer and repeating steps (B.3) (B.6) to form a second doped layer vertically below said first doped layer;

8. depositing a filler material in said trench to substantially fill said trench;

9. diffusing said dopant in the first and second doped layers to cause the first and second doped layers to overlap one another; and

C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween,

wherein said material filling the trench is high resistivity polysilicon.

17. (Currently Amended) A power semiconductor device made in accordance with a method comprising the steps of:

A. providing a substrate of a first or second conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

2. forming at least one trench in said epitaxial layer;

3. depositing a barrier material along the walls of said trench;

4. implanting a dopant of a second conductivity type through the barrier material into a portion of the epitaxial layer adjacent to and beneath the bottom of said trench;

5. diffusing said dopant to form a first doped layer in said epitaxial layer;

6. removing the barrier material from at least the bottom of the trench;

7. etching the trench through said first doped layer and repeating steps (B.3) (B.6) to form a second doped layer vertically below said first doped layer;

8. depositing a filler material in said trench to substantially fill said trench;

9. diffusing said dopant in the first and second doped layers to cause the first and second doped layers to overlap one another; and

C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween,

wherein said power semiconductor device is selected from the group consisting of a vertical Double-diffused Metal Oxide Semiconductor (DMOS), a V-groove Double-diffused Metal Oxide Semiconductor (DMOS), and a trench Double-diffused Metal Oxide Semiconductor (DMOS) Metal Oxide Semiconductor Field-Effect Transistor (MOSFET), an Insulated Gate Bipolar Transistor (IGBT), and a bipolar transistor.

18. (Currently Amended) A power semiconductor device comprising:

a substrate of a first or second conductivity type;

a voltage sustaining region disposed on said substrate, said voltage sustaining region including:

an epitaxial layer having a first conductivity type;

at least one trench located in said epitaxial layer;

at least one doped column having a dopant of a second conductivity type, said column being formed from a plurality of doped layers diffused into one another, said doped layers being located in said epitaxial layer adjacent a sidewall of said trench and arranged vertically one over the other;

a filler material substantially filling said trench; and

at least one region ~~of said second conductivity type~~ disposed over said voltage sustaining region to define a junction therebetween.

19. (Currently Amended) The device of claim 18 wherein said at least one region further includes:

a gate dielectric and a gate conductor disposed above said gate dielectric;

first and second body regions located in the epitaxial layer to define a drift region therebetween, said first and second body regions having said second conductivity type; and

first and second source regions of the first conductivity type located in the first and second body regions, respectively.

20. (Original) The device of claim 18 wherein said material filling the trench is high resistivity polysilicon.

21. (Original) The device of claim 18 wherein said material filling the trench is a dielectric material.

22. (Original) The device of claim 21 wherein said dielectric material is silicon dioxide.

23. (Original) The device of claim 21 wherein said dielectric material is silicon nitride.

24. (Original) The device of claim 18 wherein said dopant is boron.

25. (Currently Amended) The device of claim 20 wherein said first and second body regions include deep body regions.

26. (Currently Amended) The device of claim 18 wherein said trench has a circular cross-section, wherein said circular cross-section is parallel to the horizontal surface of the semiconductor device.

27. (Currently Amended) The device of claim 18 wherein said trench has a cross-sectional shape selected from the group consisting of a square, a rectangle, an octagon and a hexagon, wherein said circular cross-section is parallel to the horizontal surface of the semiconductor device.